VLSI - SYLLABUS

Advance Digital Design

- Digital Logic Fundamentals
- Combinational logic design
- Sequential logic design
- Programmable logic
- State machines

VHDL

- VHDL Overview and Concepts
- Levels of Abstraction
- Entity, Architecture
- Data Types and declaration
- Enumerated Data Types
- Relational, Logical, Arithmetic Operators
- Signal and Variables, Constants
- Process Statement
- Concurrent Statements
- When-else, With-select
- Sequential Statement
- If-then-else, Case
- Slicing and Concatenation
- Loop Statements
- Delta Delay Concept
- Arrays, Memory Modeling, FSM
- Writing Procedures
- Writing Functions
- Behavioral / RTL Coding
- Operator Overloading
- Structural Coding
- Component declarations and installations
- Generate Statement
- Configuration Block
- Libraries, Standard packages
- Local and Global Declarations
- Package, Package body
- Writing Test Benches
- Assertion based verification
- Files read and write operations
- Code for complex FPGA and ASICs
- Generics and Generic maps

VERILOG

- Language introduction
- Levels of abstraction
- Module, Ports types and declarations
- Registers and nets, Arrays
- Identifiers, Parameters
- Relational, Arithmetic, Logical, Bit-wise shift Operators
- Writing expressions
- Behavioral Modeling
- Structural Coding
- Continuous Assignments
- Procedural Statements
- Always, Initial Blocks, begin ebd, fork join
- Blocking and Non-blocking statements
- Operation Control Statements
- If, case
- Loops: while, for-loop, for-each, repeat
- Combination and sequential circuit designs
- Memory modeling,, state machines
- CMOS gate modeling
- Writing Tasks
- Writing Functions
- Compiler directives
- Conditional Compilation
- System Tasks
- Gate level primitives
- User defined primitives
- Delays, Specify block
- Testbenchs, modeling, timing checks
- Assertion based verification
- Code for synthesis
- Advanced topics
- Writing reusable code

FPGA Flow

- Re-configurable Devices, FPGA's/CPLD's
- Architectures of XILINX, ALTERA Devices
- Designing with FPGAs
- FPGA's and its Design Flows
- Architecture based coding
- Efficient resource utilization
- Constrains based synthesis
- False paths and multi cycle paths
- UCF file creation
- Timing analysis/Floor Planning
- Place and route/RPM
- Back annotation, Gate level simulation, SDF Format
- DSP on FPGA
- Writing Scripts
- Hands on experience with industry Standard Tools

VLSI Syllabus

ASIC Flow

- EDA Tools / CAD Flow for IC Design
- Simulation/Synthesis using ASIC libraries
- Clock Tree Synthesis
- False paths / Multi cycle paths / Critical paths
- Design for Testability (DFT)
- Scan Insertion / Types of Scan
- Fault Models
- Logic BIST, Memory BIST, ATGP, Boundary Scan
- Pattern Compression
- Scan Diagnostics
- Layout Design
- Placing and Routing
- LVS/DRC/OPC/Physical verification
- Diagnosis, DFM, Yield Analysis
- SOC Design and Trade-offs
- Future Trends and challenges
- ASIC Case Studies

Synthesis Concepts

Timing analysis